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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
RASHIDIAN, MOHAMMAD M	
ART UNIT	PAPER NUMBER
2624	
MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/775,652	BIDNUR ET AL.	
	Examiner	Art Unit	
	MEHDI RASHIDIAN	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *15,19 and 20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 16-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/11/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Request for Continues Examination

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 9, 2008, has been entered.

Response to Amendments/Arguments

2. Applicant's arguments filled on 10/09/2008 have been fully considered but they are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. **Claims 1-14, and 16-18** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject

matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The limitation "wherein the video decoder at least performs picture level processing" in lines 4 **of claim 1** and "wherein the video decoding the video data is discrete from the host processor in lines 12-13 of **claim 1,** and line 5 of **claim 8** are not disclosed anywhere in the specification as originally filled; Specification's paragraph [0022], line 4-7 refers to "The circuit comprises a video decoder 209, a host processor 290…" is contradicting claim limitation "discrete from host processor" in **claim 1** lines 12-13, **claim 8**, line 5, and **claim 14**, line 10. The specification as originally filed never disclosed that the decoder and host processor are discrete from each other in the circuit nor disclosed any reasons or advantages for such configuration.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. **Claims 1-14, and 16-18** are rejected under 35 U.S.C. 102(e) as being anticipated by MacInnis et al. (US PGPub 2003/0185306) henceforth referred to as MacInnis.

Regarding **Claim1**, MacInnis teaches, a system for decoding video data encoded with a particular standard, said system comprising: a video decoder for decoding the video data encoded with the particular standard, wherein the video decoder at least performs picture level processing (figs. 4a, elements 302 and 306, abstract, paragraphs [00082], [0011],…encoding/ decoding standards…, paragraphs [0042] – [0043]),

- instruction memory for storing: a first set of instructions for decoding encoded video data according to a first encoding standard, (fig. 1, abstract, paragraph [0065] first encoding/ decoding format…),
- and a second set of instruction for decoding encoded video data according to a second encoding standard, (fig. 1, abstract, paragraph [0065] second encoding/ decoding format…),
- a host processor for providing an indication to the video decoder indicating the particular encoding standard, wherein the video decoder for decoding the video data encoded with the particular standard and at least performing picture level processing, is discrete from the host processor, (fig. 3, paragraph [0044, lines 1-10], and paragraph [0040, lines 1-11], and paragraph [0030, lines 4-10], and paragraph [0031, lines 1-10] …first decoder controls processor…, paragraph

[0083, last 14 lines] system 300 of fig. 3 provides…, decoding standards…, paragraph [0042] – [0043]),

- and wherein the video decoder executes the first set of instructions if the indication indicates that the particular encoding standard is the first encoding standard and executes the second set of instructions if the indication indicates that the particular encoding standard is the second encoding standard, (figs. 1-3, abstract, paragraph [0011])

Regarding **Claim 2**, MacInnis teaches, the system of **claim 1**, wherein the first encoding standard comprises MPEG-2 and the second encoding standard comprises MPEG-4, (figs. 1-3, abstract, paragraph [0026] MPEG-1, MPEG-2,…MPEG-4).

Regarding **Claim 3**, MacInnis teaches, the system of **claim 1**, wherein the instruction memory stores a third set of instructions for decoding encoded video data according to a third encoding standard, and wherein the video decoder executes the third set of instructions if the indication indicates that the particular encoding standard is the third encoding standard, (figs. 3, abstract, paragraph [0056-0058] processor 300…).

Regarding **Claim 4**, MacInnis teaches, the system of **claim 3**, wherein the first encoding standard comprises MPEG-2, the second encoding standard comprises MPEG-4, and the third encoding standard comprises DV-25, (figs. 6, abstract, paragraph [0083] Digital Video).

Regarding **Claim 5**, MacInnis teaches, the system of **claim 3**, wherein the instruction memory stores a fourth set of instructions for decoding the video data in accordance with the first encoding standard, the second encoding standard, and the third encoding standard, (figs. 6, abstract, paragraph [0083] Digital Video…).

Regarding **Claim 6**, MacInnis teaches, the system of **claim 1**, further comprising a register for storing the indication from the host processor, (paragraph [0031] each hardware module includes the status register…).

Regarding **Claim 7**, MacInnis teaches, the system of **claim 6**, wherein the instruction memory stores a fifth set of instructions, wherein execution of the instructions by the host processor cause: detecting the particular encoding standard; and writing the indicator to the register. (paragraph [0031] each hardware module includes the status register…).

Regarding **Claim 8**, MacInnis teaches, a method for decoding video data encoded with a particular standard, said method comprising: receiving an indication from host processor by a video decoder indicating the particular encoding standard, wherein the video decoder at least performs picture level processing and is discrete from the host processor, (figs. 4a, elements 302 and 306, abstract, paragraph [002], …encoding/ decoding standards… , paragraph [0042] – [0043]),

- executing a first set of instructions if the indication indicates that the particular encoding standard is a first encoding standard, (fig. 1, abstract, paragraph [0065] first encoding/ decoding format…),
- and executing a second set of instructions if the indication indicates that the particular encoding standard is the second encoding standard, (fig. 1, abstract, paragraph [0065] second encoding/ decoding format…, paragraph [0083, last 14 lines] system 300 of fig. 3 provides…).

Regarding **Claim 9**, MacInnis teaches, the method of **claim 8**, wherein the first encoding standard comprises MPEG-2 and the second encoding standard comprises MPEG-4, (figs. 1-3, abstract, paragraph [0026] MPEG-1, MPEG-2,…MPEG-4).

Regarding **Claim 10**, MacInnis teaches, the method of **claim 8**, further comprising executing the third set of instructions if the indication indicates that the particular encoding standard is the third encoding standard, (figs. 3, abstract, paragraph [0056-0058] processor 300…).

Regarding **Claim 11**, MacInnis teaches, the method of **claim 10**, wherein the first encoding standard comprises MPEG-2, the second encoding standard comprises MPEG-4, and the third encoding standard comprises DV-25, (figs. 6, abstract, paragraph [0083] Digital Video).

Regarding **Claim 12**, MacInnis teaches, the method of **claim 10**, executing a fourth set of instructions for decoding the video data in accordance with the first encoding standard, the second encoding standard, and the third encoding standard, (figs. 6, abstract, paragraph [0083] Digital Video…).

Regarding **Claim 13**, MacInnis teaches, the method of **claim 8**, further comprising: detecting the particular encoding standard; and writing the indicator to a register, (paragraph [0031] each hardware module includes the status register…).

Regarding **Claim 14**, MacInnis teaches, a system for decoding video data encoded with a particular standard, said system comprising: a code memory for instructions; and a processor for loading the code memory with a first set of instructions for decoding encoded video data according to a first encoding standard, (fig. 3, paragraph [0044, lines 1-10], and paragraph [0040, lines 1-11], and paragraph [0030, lines 4-10], and paragraph [0031, lines 1-10] …first decoder controls processor…),

- where the video data is encoded according to the first encoding standard and for loading the code memory a second set of instruction for decoding encoded video data according to a second encoding standard, (fig. 1, abstract, paragraph [0065] first encoding/ decoding format…),

- wherein the video data is encoded according to the second encoding standard. (fig. 1, abstract, paragraph [0065] second encoding/ decoding format…, paragraph [0083, last 14 lines] system 300 of fig. 3 provides…),
- wherein the processor loads the code memory after receiving an indication from a discrete host processor indicating the particular encoding standard, (fig. 4a, paragraph [0044, lines 1-10], and paragraph [0040, lines 1-11], and paragraph [0030, lines 4-10], and paragraph [0031, lines 1-10] …first decoder controls processor…, paragraph [0083, last 14 lines] system 300 of fig. 3 provides…, decoding standards…, fig 4a, elements 302 and 306, paragraph [0042] – [0043]).

Regarding **Claim 16**, MacInnis teaches, the system of **claim 14**, wherein execution of the first set of instructions by the processor controls a first plurality of circuits, and execution of the second set of instructions controls a second plurality of circuits. (figs. 1-3, abstract, paragraph [0026] MPEG-1, MPEG-2,…MPEG-4).

Regarding **Claim 17**, MacInnis teaches, the system of **claim 14**, further comprising a slave engine, said slave engine further comprising: another instruction memory for storing a third set of instructions if the encoding standard is the second encoding standard, (figs. 3, abstract, paragraph [0056-0058] processor 300…).

Regarding **Claim 18**, MacInnis teaches, the system of **claim 17**, wherein the slave engine comprises a third plurality of circuits, wherein the execution of the third set of instructions controls the third plurality of circuits, (figs. 3, abstract, paragraph [0056-0058] processor 300…).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MEHDI RASHIDIAN whose telephone number is (571)272-9763. The examiner can normally be reached on Mon-Thurs 9:00AM to 8:00PM, ET.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Samir Ahmed can be reached on (571) 272-7413. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Mehdi Rashidian/
Examiner, Art Unit 2624
12/18/2008

/Samir A. Ahmed/
Supervisory Patent Examiner, Art Unit 2624